IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) An electronic assembly comprising:

a substrate;

a die;

a plurality of interconnections between the substrate and die;

wherein respective ones of the interconnections include a relatively low melting temperature and yield strength reflowed solder bump on the die, a relatively higher melting temperature and electrically conductive material standoff on the substrate in the form of a stiff bump extending above the substrate surface and having a yield strength in the 350-450 MPa range, and a soldered joint connecting the reflowed solder bump to the electrically conductive material standoff.

2. (Canceled)

3. (Previously Presented) The electronic assembly according to claim 1, wherein the top surface of the standoff is wetted by the reflowed solder bump to form the soldered joint.

4. (Previously Presented) The electronic assembly according to claim 1, wherein the standoff is a bump in the form of a column or stud.

5. (Previously Presented) The electronic assembly according to claim 1, wherein the relatively higher melting temperature and electrically conductive material standoff is copper.

6. (Canceled)

7. (Original) The electronic assembly according to claim 1, wherein the die has an inter layer dielectric material under the interconnections.

8. (Canceled)

9. (Original) The electronic assembly according to claim 1, wherein the coefficient of thermal expansion of the substrate is at least 15 ppm/°C and the coefficient of thermal expansion of the die is at least 2.7 ppm/°C less than that of the substrate.

10. (Original) The electronic assembly according to claim 1, wherein the coefficient of thermal expansion of the substrate is more than two times greater than the coefficient of thermal expansion of the die.

11. (Previously Presented) A semiconductor package comprising:

a package substrate having a coefficient of thermal expansion of at least 15 ppm/°C, the package substrate having a plurality of relatively high melting temperature and electrically conductive standoff contact members on the substrate;

a die having a coefficient of thermal expansion which is at least 2.7 ppm/°C less than that of the substrate, a front side of the die having a plurality of relatively lower yield strength reflowed solder bumps thereon, the die being located on the substrate with the solder bumps connected to the respective ones of the standoff contact members by soldered joints electrically coupling the die to the substrate.

12. (Original) The semiconductor package according to claim 11, wherein the coefficient of thermal expansion of the substrate is more than twice that of the die.

13. (Previously Presented) The semiconductor package according to claim 12, wherein the standoff contact members comprise a plurality of standoff elements upstanding from a surface of the substrate, and wherein the soldered joints connect the die to the tops of respective ones of the standoff elements.

14. (Original) The semiconductor package according to claim 13, wherein the standoff elements are non-melting at the solder liquidous temperature.

15. (Original) The semiconductor package according to claim 13, wherein the standoff elements are copper bumps.

16. (Original) The semiconductor package according to claim 13, wherein the soldered joints each comprise solder on the die which is wetted onto a surface of a contact member of the substrate to form the soldered joint.

17. (Original) The semiconductor package according to claim 11, wherein the die has an inter layer dielectric material under the solder connections thereon.

18. (Canceled)

19. (Withdrawn) A method of interconnecting a die and substrate to one another for reduced die stresses, the method comprising:

providing a relatively low melting temperature and yield strength solder bump on a die and a relatively higher melting temperature and electrically conductive material standoff contact member on a substrate; and

reflow soldering the solder bump to form a soldered joint connecting the solder bump to the electrically conductive material standoff contact member.

20. (Canceled)

21. (Withdrawn) The method according to claim 19, wherein the solder bump is wetted on the top surface of the standoff contact member to form the soldered joint.

22 (Withdrawn) The method according to claim 19, wherein the solder bump is provided over an inter layer dielectric material in the die.

23. (Canceled)

24. (Withdrawn) The method according to claim 19, wherein the coefficient of thermal expansion of the substrate is at least 15 ppm/°C and the coefficient of thermal expansion of the die is at least 2.7 ppm/°C less than that of the substrate.

25. (Withdrawn) The method according to claim 19, wherein the reflow soldering includes separately heating the die and solder bump to at least a soldering temperature and thereafter contacting the solder bump with the standoff contact member on the substrate for forming the soldered joint.

26. (Withdrawn) The method according to claim 25, further comprising separately heating the substrate to a temperature substantially lower than the reflow soldering temperature before contacting the solder bump on the die with the standoff contact member on the substrate to form the soldered joint.

NEW CLAIMS:

27. (New) A semiconductor package comprising:

a package substrate having a plurality of relatively high melting temperature and electrically conductive standoff contact members on the substrate in the form of a stiff bump extending above a substrate surface and having a yield strength in the 350-450 MPa range; and

a die having a front side with a plurality of relatively low melting temperature and yield strength reflowed solder bumps thereon, the die capable of being coupled to the substrate with the solder bumps connected to the respective ones of the standoff contact members by soldered joints electrically coupling the die to the substrate.